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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,173	02/03/2006	Joseph M. Amato	US03 0199 US2	9635
65913	7550	10/28/2008		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131				
EXAMINER				
LEE, HSIEN MING				
ART UNIT		PAPER NUMBER		
2823				
NOTIFICATION DATE		DELIVERY MODE		
10/28/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/567,173

Applicant(s)

AMATO, JOSEPH M.

Examiner

Hsien-ming Lee

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 22-25 is/are allowed.
- 6) ☒ Claim(s) 1, 14, 15, 19 and 20 is/are rejected.
- 7) ☒ Claim(s) 2-13, 16-18 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 20080730
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claim 3 is objected to because of the following informalities: at line 3, the term "structure" repeats twice. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

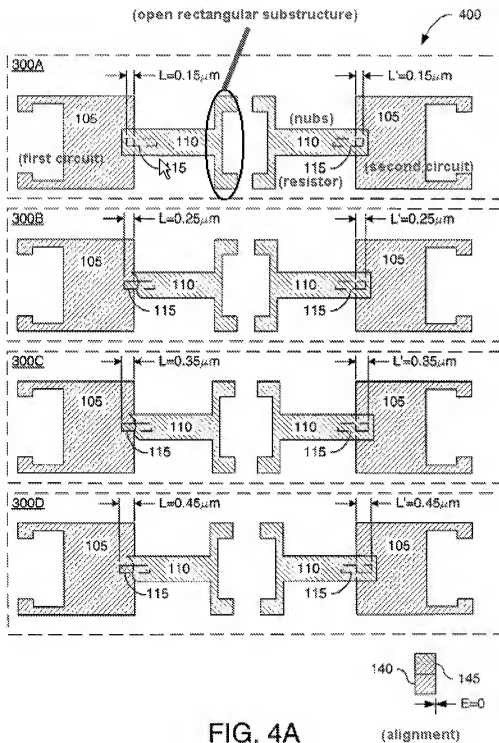
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 14 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Look et al. (US 2001/0049881, submitted by applicant).

In re claim 1, Look et al, in Figs. 4A, 5A and corresponding text, teach a method for identifying misalignments in an overlapping region of a stitched circuit in an integrated circuit fabrication process, comprising:

- creating a first circuit 105 (the one the left) using a reference mask, wherein first circuit 105 includes a first part of an offset dependent resistor structure 115 in the overlapping region (Fig.4A);

- creating a second circuit 105 (the one on the right) using a secondary mask, wherein the second circuit 105 includes a second part of the offset dependent resistor structure 115 in the overlapping region, wherein the offset dependent resistor structure 115 includes a plurality of nubs 110 that interconnect the first part and the second part of the offset dependent resistor structure 115 (Fig.4A);
- measuring a resistance across the offset dependent resistor structure (paragraph [0045]); and
- determining an amount of misalignment based on the measured resistance (paragraphs [0043], [0045], [0055], [0056]).



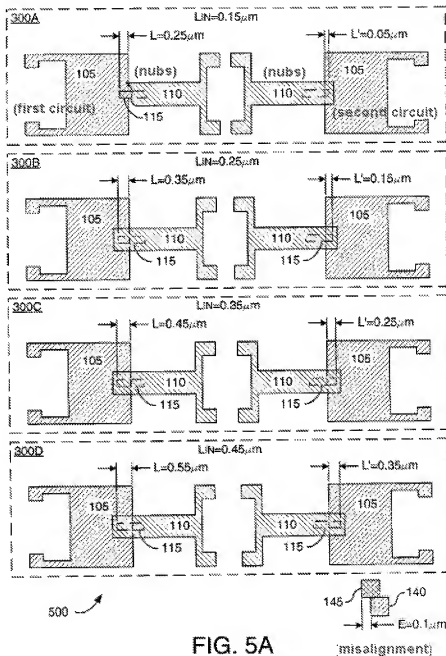


FIG. 5A

In re claim 14, Look et al. teach an offset dependent resistor structure for identifying a misalignment in an overlapping region of a stitched portion of an integrated circuit, comprising:

- * a first part of an offset dependent resistor structure 115 (i.e. the one on the left) created in the overlapping region using a reference mask (Figs. 4A and 5A);
- * a second part of the offset dependent resistor structure 115 (i.e. the one on the right) superimposed on the first part in the overlapping region using a secondary mask; and a plurality of nubs 110 that interconnect the first part and the second part of the offset dependent resistor structure 115 to form a single electrical pathway (Figs. 4A and 5A), wherein the resistance of the single electrical pathway is dependent upon the length of the nubs 110 that interconnect the first part and the second part of the offset dependent resistor structure 115 (see Fig.4B and 5B).

In re claim 19, Look et al., in Figs. 4A and 5A and corresponding text, a system for measuring misalignments in an overlapping region of a stitched portion of an integrated circuit, comprise:

- * an offset dependent resistor structure 115, including: a first part 105 (the one on the left) created in the overlapping region using a reference mask, a second part 105 (the one on the right) superimposed on the first part in the overlapping region and created using a secondary mask; and
- * a plurality of nubs 110 oriented in a first uniform direction that interconnect the first part and the second part to form a single electrical pathway, wherein the resistance

of the single electrical pathway is dependent upon the length of the hubs 110 (see Figs. 4B and 5B) that interconnect the first part and the second part, and a system for measuring the resistance across the single electrical pathway (paragraphs [0043], [0045], [0055], [0056].

4. Claims 1, 14, 15, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US 6,323,097, submitted by applicant).

In re claim 1, Wu et al, in Fig. 7 and corresponding text, teach a method for identifying misalignments in an overlapping region of a stitched circuit in an integrated circuit fabrication process, comprising:

- creating a first circuit 90 using a reference mask, wherein first circuit 90 includes a first part of an offset dependent resistor structure 96 in the overlapping region;
- creating a second circuit 86 using a secondary mask, wherein the second circuit 86 includes a second part of the offset dependent resistor structure 96 in the overlapping region, wherein the offset dependent resistor structure 96 includes a plurality of nubs 96 that interconnect the first part and the second part of the offset dependent resistor structure 96;
- measuring a resistance across the offset dependent resistor structure (col. 6, lines 33-57); and

- determining an amount of misalignment based on the measured resistance (col. 6, line 65 through col. 7, line 2).

In re claim 14, Wu et al., in Fig.7 and corresponding text, teach an offset dependent resistor structure for identifying a misalignment in an overlapping region of a stitched portion of an integrated circuit, comprising:

- * a first part of an offset dependent resistor structure (94/96 on the left side of 92) created in the overlapping region using a reference mask;
- * a second part of the offset dependent resistor structure (94/96 on the right side of 92) superimposed on the first part in the overlapping region using a secondary mask; and a plurality of nubs 96 that interconnect the first part and the second part of the offset dependent resistor structure 94/94 to form a single electrical pathway, wherein the resistance of the single electrical pathway is dependent upon the length of the nubs 96 that interconnect the first part and the second part of the offset dependent resistor structure 94/96.

In re claim 15, Wu et al., in Fig.7 and corresponding text, teach comprising a pair of test pads 100 and 102 at ends of the single electrical pathway.

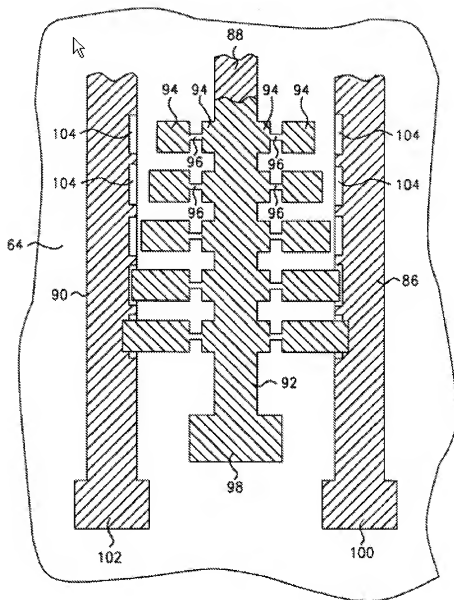


FIG. 7

In re claim 19, Wu et al., in Fig. 7 and corresponding text, a system for measuring misalignments in an overlapping region of a stitched portion of an integrated circuit, comprise:

- * an offset dependent resistor structure, including: a first part 102 created in the overlapping region using a reference mask, a second part 100 superimposed on the first part in the overlapping region and created using a secondary mask; and
- * a plurality of nubs 96 oriented in a first uniform direction that interconnect the first part 102 and the second part 100 to form a single electrical pathway, wherein the resistance of the single electrical pathway is dependent upon the length of the hubs 96 that interconnect the first part 102 and the second part 100, and a system for measuring the resistance across the single electrical pathway (col. 6, lines 33-57 and col. 6, line 65 through col. 7, line 2).

In re claim 20, Wu et al., in Fig.7 and corresponding text, teach that the system for measuring the resistance comprises a pair of test pads 100 and 102 at ends of the single electrical pathway and a pair of probes.

Response to Arguments

5. Applicant's arguments filed 7/30/08 have been fully considered and are persuasive. The restriction has been withdrawn. Claims 1-25 are treated on their merits in this office action.

Allowable Subject Matter

6. Claims 22-25 are allowed.
7. Claims 2-13, 16-18 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. The following is a statement of reasons for the indication of allowable subject matter:

In re claim 2, none of the prior art of record, teaches or suggests that the other part of the offset dependent resistor structure comprises three substructures that interconnect with the open terminal points of the rectangular substructures to form a single electrical pathway when the first and second parts are superimposed.

In re claim 8, none of the prior art of record, teaches or suggests that one of the parts of the offset dependent resistor structure comprises a pair of open E-shaped substructures and other part of the offset dependent resistor structure comprises three substructures.

In re claim 16, none of the prior art of record, teaches or suggests that the second part of the offset dependent resistor structure comprises three substructures that interconnect with the open terminal points of the open rectangular substructures to form a single electrical pathway.

In re claim 17, none of the prior art of record, teaches or suggests that the second part of the offset dependent resistor structure comprises three substructures

that interconnect with the open terminal points of the E-shaped substructures to form a single electrical pathway.

In re claim 18, none of the prior art of record, teaches or suggests that the first part and the second part of the offset dependent resistor structure interconnect via four nubs.

In re claim 21, none of the prior art of record, teaches or suggests a plurality of second nubs oriented in a second uniform direction that interconnect the first part and the second part to form a single electrical pathway, wherein the second uniform direction is perpendicular to the first uniform direction.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Monday through Friday (8:30 ~ 17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hsien-ming Lee/
Primary Examiner
Art Unit 2823

Oct. 13, 2008